REMARKS

The Office Action of May 17, 2006, has been received and reviewed.

Claims 1-22 are currently pending and under consideration in the above-referenced application, each standing rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections under 35 U.S.C. § 102

Claims 1-10, 13-17, and 18-22 stand rejected under 35 U.S.C. § 102.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Bertin

Claims 1-10 and 13-17 are rejected under 35 U.S.C. § 102(b) for being drawn to subject matter that is allegedly anticipated by the subject matter described in U.S. Patent 5,977,640 to Bertin et al. (hereinafter "Bertin").

Bertin describes, among other things, assemblies that include chips 30 and 40, such as a logic device and a memory device, that face one another and are electrically connected to each other. *See, e.g.,* FIGs. 1 and 6; col. 4, lines 20-37. A larger of the chips 40 may also be electrically connected to an interposer 32, while the smaller of the chips 30 may be received within a receptacle of the interposer 32. *See, e.g.,* FIGs. 1 and 6.

While Bertin explains that the two chips 30 and 40 may be electrically connected to one another, Bertin does not expressly or inherently describe that either chip 30 or 40 includes "conductive members . . .including laterally extending portions that are at least partially carried by a surface" thereof. As such, Bertin does not anticipate each and every element of the method recited in independent claim 1, as amended and presented herein, as would be required to maintain the 35 U.S.C. § 102(b) rejection of independent claim 1.

Each of claims 2-10 and 13-17 is allowable, among other reasons, for depending directly or indirectly from amended independent claim 1, which is allowable.

Oka

Claims 18, 19, 21, and 22 stand rejected under 35 U.S.C. § 102(e) for reciting subject matter which is assertedly anticipated by the subject matter described in U.S. Patent 6,441,495 to Oka et al. (hereinafter "Oka").

The description of Oka relates to processes for securing leads to semiconductor devices. One of these processes is tape-automated bonding (TAB), in which the leads that are carried by a polymeric film (tape) are electrically connected to bond pads of a semiconductor die. FIGs. 17 and 18 of Oka illustrate the TAB process, which is described more fully in columns 13 and 14 of Oka. Polymeric tape is not substantially rigid.

As currently amended, independent claim 18, in the relevant part recites, "[a] method for assembling semiconductor device components, comprising: providing an interposer with a substantially planar, *substantially rigid* substrate and a receptacle formed substantially through the substrate..."

Again, the polymeric tape disclosed by Oka is not substantially rigid. As such, Oka does not expressly or inherently describe each and every element of the method of amended independent claim 18. Therefore, the method of amended independent claim 18 is, under 35 U.S.C. § 102(b), allowable over the subject matter described in Oka.

Claims 19, 21, and 22 are each allowable, among other reasons, for depending directly or indirectly from allowable claim 18.

Claim 22 is also allowable since Oka neither expressly nor inherently describes positioning a semiconductor device that includes a redistribution circuit. In fact, Oka lacks any mention of a semiconductor device with a redistribution circuit.

It is respectfully requested that the 35 U.S.C. § 102 rejections of claims 1-10 and 13-22 be withdrawn, and that each of these claims be allowed.

Rejections under 35 U.S.C. § 103(a)

Claims 1, 2, 7, 8, 11, 12, and 18-22 have been rejected under 35 U.S.C. § 103(a).

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Urishima in View of Park

Claims 1, 2, 7, 8, 11, and 12 are rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in U.S. Patent 6,791,195 to Urushima et al. (hereinafter "Urushima"), in view of teachings from U.S. Patent Publication 2001/0004128 of Park et al. (hereinafter "Park").

The relevant teachings of Urushima, which are depicted in FIG. 11A, relate to assembly methods that include interconnecting a semiconductor device 3d with two other semiconductor devices 3c and 3e that are located in substantially the same plane. *See also,* col. 20, lines 5-56. Solder balls 21 electrically connect bond pads of semiconductor device 3d to corresponding bond pads of semiconductor devices 3c and 3e. *See id.* When such an assembly is oriented with respect to an interposer 48, semiconductor device 3d is received within a hole 51 of the interposer 48. *See id.* Bond pads of the other semiconductor devices 3c and 3e are electrically connected to corresponding conductors of the interposer 48 by way of solder balls 21. *See id.*

Park teaches that a tape 50 may be placed on a surface of a circuit board 10 so as to cover an aperture 15 of the circuit board. *See, e.g.,* FIGs. 2A and 2B. The tape 50 supports a semiconductor chip 2 positioned within the aperture 15 in such a way as to position a back side

of the semiconductor chip 2 in substantially the same plane as the surface of the circuit board 10 to which the tape 50 is adhered. *See id.*

It is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 1, 2, 7, 8, 11, and 12. For example, with respect to the subject matter recited in amended independent claim 1, it is respectfully submitted that neither Urushima nor Park teaches or suggests "electrically connecting the at least one first-level semiconductor device to at least the conductors on the upper surface of the substrate by first-level conductive members that include laterally extending portions that are at least partially carried by a surface of the second-level semiconductor device."

Therefore, it is respectfully submitted that, under 35 U.S.C. § 103(a), the subject matter to which amended independent claim 1 is directed is allowable over the subject matter taught in Urushima and Park.

Each of claims 2, 7, 8, 11 and 12 is allowable, among other reasons, for depending directly or indirectly from amended independent claim 1, which is allowable.

Oka in View of Chia

Claims 18-22 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Oka, in view of teachings from U.S. Patent 5,841,191 to Chia et al. (hereinafter "Chia").

The teachings of Oka relate to processes for securing leads to semiconductor devices. One of these processes is tape-automated bonding (TAB), in which the leads that are carried by a polymeric film (tape) are electrically connected to bond pads of the semiconductor die. FIGs. 17 and 18 of Oka illustrate the TAB process, which is described more fully in columns 13 and 14 of Oka.

Chia describes a ball grid array package with compact wire bond interconnections. Col. 1, lines 1-4. The package may be formed on a substantially rigid TAB substrate. Col. 1, lines 18-21.

Neither Oka nor Chia teaches or suggests that, upon "electrically connecting at least the first semiconductor device to the interposer," the second semiconductor device is also electrically

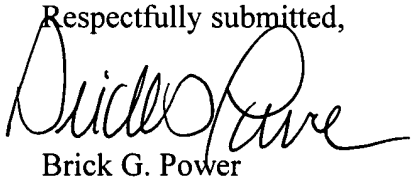
connected to the interposer by "at least a laterally extending portion of at least one conductive element carried by a surface of the first semiconductor device . . .," as recited in independent claim 18, as amended and presented herein. Therefore, the teachings of Oka and Chia do not support a *prima facie* case of obviousness against amended independent claim 18 or against any of claims 19-22 depending directly or indirectly therefrom. Accordingly, under 35 U.S.C. § 103(a), the subject matter recited in claims 18-22 is allowable over the subject matter taught in Oka and Chia.

Withdrawal of the 35 U.S.C. § 103(a) rejections of claims 1, 2, 7, 8, 11, 12, and 18-22 is respectfully requested, as is the allowance of each of these claims.

CONCLUSION

It is respectfully submitted that each of claims 1-22 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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